In the Claims

Claims

Claims 1-50 (Canceled).

51. (Previously presented) A method of forming a transistor gate comprising:

forming a gate oxide layer over a semiconductive substrate;

providing fluorine within the gate oxide layer;

forming a gate proximate the gate oxide layer having the fluorine therein after the providing; and

forming at least one sidewall spacer laterally adjacent the gate and directly over the gate oxide layer, the at least one sidewall spacer comprising fluorine for the providing.

52. (Previously presented) The method of claim 51 wherein the fluorine is provided in the gate oxide layer to a concentration of from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

53. (Previously presented) The method of claim 51 wherein the gate comprises opposing lateral edges and a central region therebetween, the fluorine being provided within the gate oxide layer to a greater concentration proximate at least one of the gate edges than in the central region.

Claim 54 (Canceled).

55. (Withdrawn) A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a center therebetween, the gate oxide layer having a center and outwardly exposed opposing edges laterally aligned with the edges of the gate;

concentrating at least one of chlorine or fluorine in the gate oxide layer having the outwardly exposed opposing edges and within the overlap more proximate at least one of the outwardly exposed oxide gate edges than the center; and

after the concentrating, forming sidewall spacers proximate the opposing edges of the gate and the gate oxide, the spacers being substantially devoid of fluorine.

56. (Withdrawn) The method of claim 55 wherein the concentrating comprises concentrating fluorine.

57. (Withdrawn) The method of claim 55 wherein the gate is formed to have a gate width between the edges of 0.25 micron or less, the concentrating forming at least one concentration region in the gate oxide which extends laterally inward from the at least one gate edge no more than about 500 Angstroms.

58. (Withdrawn) The method of claim 55 wherein the concentrating comprises diffusion doping.

59. (Withdrawn) The method of claim 55 wherein the concentrating comprises ion implanting.

Claims 60 and 61 (Canceled).

62. (Previously presented) A method of forming a transistor gate comprising:

forming a gate and a gate oxide layer in overlapping relation, the gate having opposing edges and a central region therebetween;

forming sidewall spacers comprising at least one of the chlorine or fluorine proximate the opposing edges and directly elevationally over the gate oxide layer; and

doping the gate oxide layer within the overlap with at least one of chlorine or fluorine proximate the opposing gate edges and leaving the central region substantially undoped with chlorine and fluorine.

63. (Previously presented) The method of claim 62 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

64. (Previously presented) The method of claim 62 further comprising removing portions of the gate oxide layer not overlapping the gate.

65. (Previously presented) The method of claim 62 wherein the doping comprises diffusion doping at least one of chlorine or fluorine from the spacers into the gate oxide layer.

66. (Previously presented) The method of claim 65 further comprising annealing the spacers to provide the diffusion doping.

67. (Previously presented) The method of claim 62 wherein the doping comprises doping with fluorine.

68. (Previously presented) A method of forming a transistor gate comprising the following sequential steps:

forming a gate over a gate oxide layer, the gate having opposing lateral edges and the gate oxide layer provided elevationally below the gate and extending laterally past the lateral edges of the gate;

forming sidewall spacers comprising at least one of chlorine or fluorine proximate the opposing lateral edges; and

diffusion doping at least one of chlorine or fluorine into the gate oxide layer beneath the gate from laterally outward of the gate edges.

69. (Previously presented) The method of claim 68 wherein the doping provides a dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

70. (Previously presented) The method of claim 68 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms.

71. (Previously presented) The method of claim 68 wherein the doping provides a pair of spaced and opposed concentration regions in the gate oxide which extend laterally inward from the gate edges no more than about 500 Angstroms, the concentration regions having an average dopant concentration in the gate oxide layer proximate the edges from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3.

72. (Previously presented) The method of claim 71 wherein the gate oxide layer between the concentration regions is substantially undoped with chlorine and fluorine.

73. (Previously presented) The method of claim 68 further comprising removing portions of the gate oxide layer not beneath the gate.

74. (Previously presented) The method of claim 68 wherein the diffusion doping comprises annealing the sidewall spacers.

75. (Previously presented) The method of claim 68 wherein the diffusion doping comprises diffusion doping fluorine.

Claims 76-78 (Currently Canceled).

79. (Withdrawn) The method of claim 55 wherein the concentrating the at least one of chlorine or fluorine provides a concentration of chlorine or fluorine which effective to diminish hot carrier effects.

80. (Previously presented) The method of claim 62 wherein the doping the gate oxide layer with the at least one of chlorine or fluorine provides a concentration of chlorine or fluorine effective to diminish hot carrier effects.

81. (Previously presented) The method of claim 68 wherein the diffusion doping the at least one of chlorine or fluorine into the gate oxide layer provides a concentration of chlorine or fluorine which effective to diminish hot carrier effects.

Claims 82-85 (Canceled).

86. (Withdrawn) The method of claim 55 wherein the sidewall spacers are formed directly over the gate oxide layer.

87. (Previously presented) The method of claim 68 wherein the sidewall spacers are formed directly over the gate oxide layer.

88. (Previously presented) A method of forming a transistor gate comprising:

forming a gate oxide layer over a semiconductive substrate;

providing fluorine within the gate oxide layer;

forming a gate proximate the gate oxide layer having the fluorine therein after the providing; and

forming at least one sidewall spacer laterally adjacent the gate and directly over the gate oxide layer.

89. (Previously presented) The method of claim 88 wherein the at least one sidewall spacer comprises fluorine for the providing.

90. (Previously presented) The method of claim 88 wherein the forming of the at least one sidewall spacer comprises forming the spacer over the gate oxide layer in a direction extending perpendicularly to a surface of the semiconductor substrate.

91. (Previously presented) The method of claim 51 further comprising providing a substrate having an upper surface, and wherein the forming of the at least one sidewall spacer comprises forming the sidewall spacer directly over the gate oxide layer in a direction extending perpendicularly to the upper surface of the substrate.

92. (Withdrawn) The method of claim 55 further comprising providing a substrate having an upper surface, and wherein the forming of the sidewall spacers comprises forming the sidewall spacers directly over the gate oxide layer in a direction extending perpendicularly to the upper surface of the substrate.

93. (Previously presented) The method of claim 62 further comprising providing a substrate having an upper surface, and wherein the forming of the sidewall spacers comprises forming the sidewall spacers directly over the gate oxide layer in a direction extending perpendicularly to the upper surface of the substrate.

94. (Previously presented) The method of claim 62 further comprising providing a substrate supporting the gate oxide layer, and wherein the gate oxide layer is provided intermediate the substrate and spacers.

95. (Previously presented) The method of claim 62 further comprising providing a substrate supporting the gate oxide layer, and wherein an entirety of the spacers is spaced from the substrate.

96. (Previously presented) The method of claim 68 wherein the forming the spacers comprises forming the spacers directly over the extending lateral portion of the gate oxide layer.

97. (Previously presented) The method of claim 68 further comprising providing a substrate supporting the gate oxide layer, and wherein an entirety of the spacers is spaced from the substrate.

98. (Previously presented) The method of claim 68 further comprising providing a substrate having an upper surface, and wherein the forming of the sidewall spacers comprises forming the sidewall spacers directly over the gate oxide layer in a direction extending perpendicularly to the upper surface of the substrate.